EOP400-FR4

400Gb/s OSFP56 FR4 2km SMF Optical Transceiver

PRODUCT FEATURES

- **Supports 425Gbps**
- **Single 3.3V Power Supply**
- **Up to 2km over SMF with KP4 FEC**
- **supported at the Host side**
- **Duplex LC connector**
- **8x53.125Gbps (PAM4) electrical interface**
- **PIN and TIA array on the receiver side**
- **Power dissipation < 8W**
- **Case temperature range: 0°C to 70°C (commercial)**
- **Safety Certification: TUV/UL/FDA*1**
- **RoHS Compliant**

APPLICATIONS

- **400G Ethernet**
- **400G-FR4 applications**
- **Data center**
- **InfiniBand**

DESCRIPTIONS

ETU-Link's OSFP transceiver module is designed for use in 400 Gigabit Ethernet links over 2km single mode fiber. The module has 8 independent electrical input/output channels operating up to 53.125Gbps per channel. The integrated GearBox in module converts the 8 channels of 53.125Gbps (PAM4) electrical input data to 4 channels of parallel optical signals, each capable of 106.25Gbps (PAM4) operation for an aggregate data rate of 400Gb/s. The four transmitter/receiver units operate on the ITU G.694.2 CWDM grid near 1300nm. The transmitter path of the module incorporates a bi-directional PAM4 re-timer ASIC integrated with a 4-channels modulator driver, 4 externally modulated lasers and one optical multiplexer. On the receiver path, an optical de-multiplexer is coupled to 4 photodiodes, along with the PAM4 re-timer that built-in 4-channel TIA array. The electrical interface of the module is compliant with the 400GAUI-8 interface as defined by IEEE 802.3bs, and compliant with OSFP MSA.

Module Block Diagram

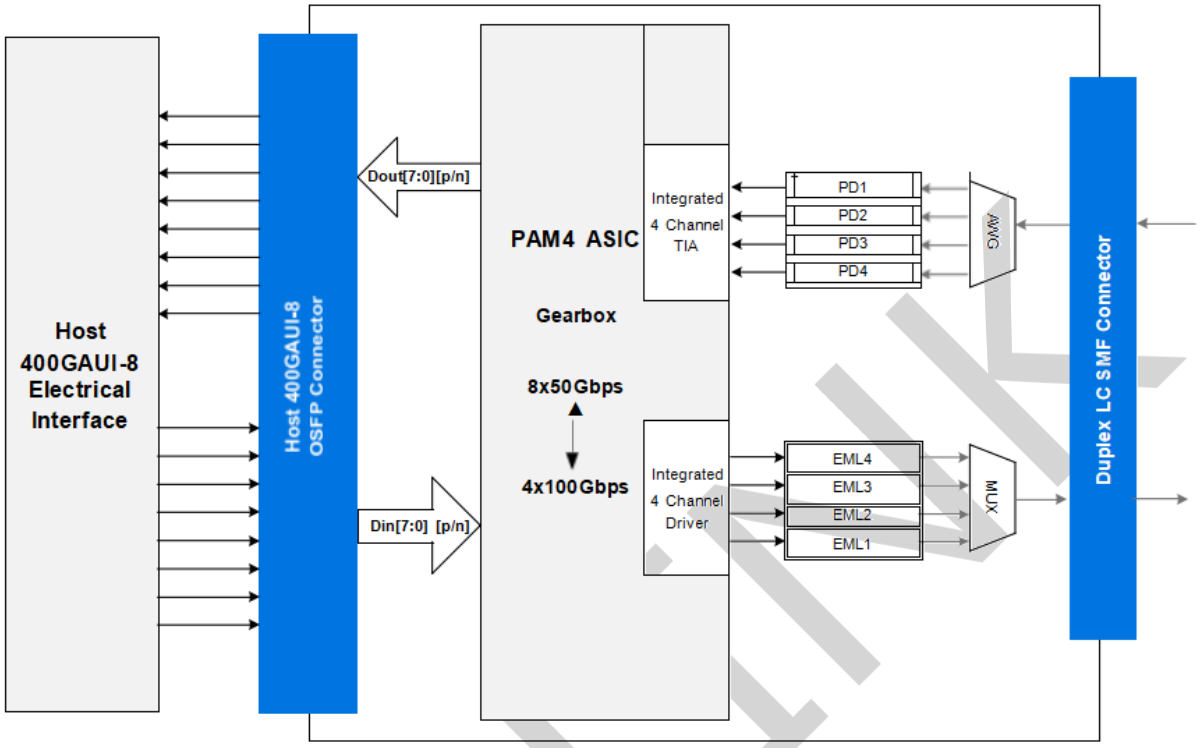


Figure 1: Transceiver Block Diagram

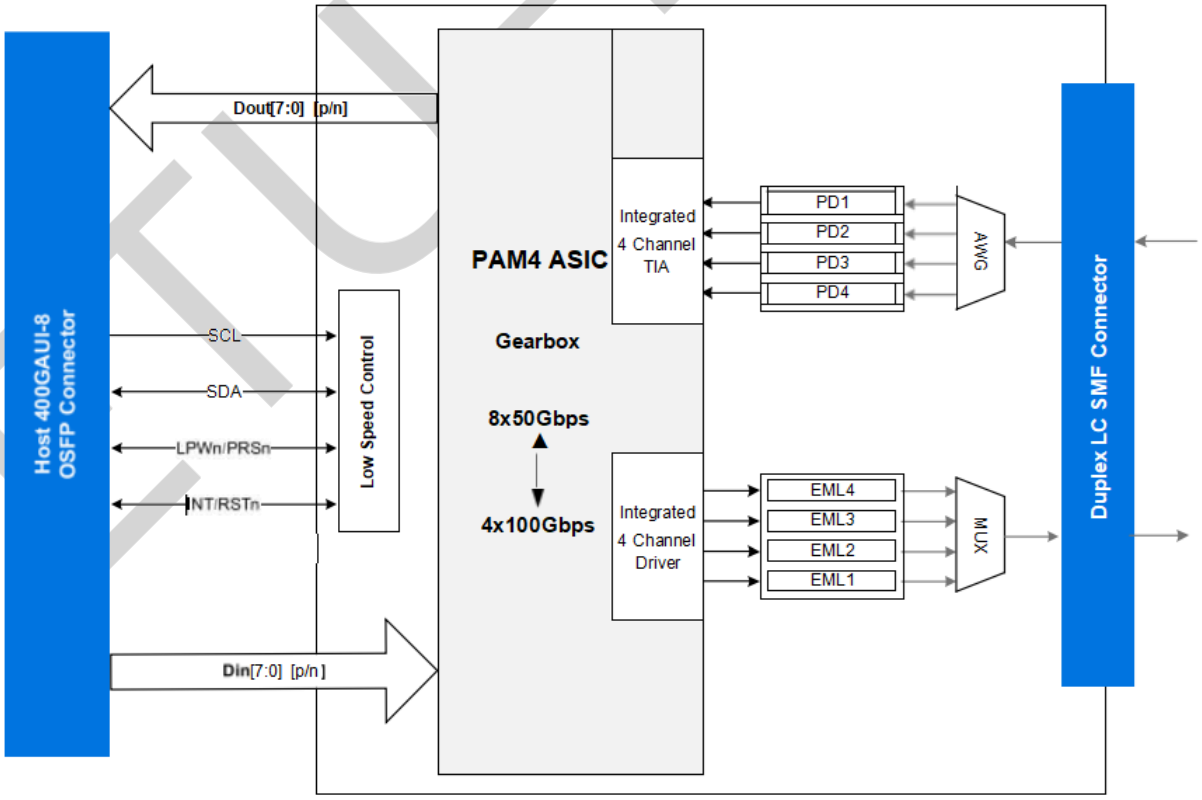


Figure 2: Application Reference Diagram

Ordering Information

Part No.	Description
EOP400-FR4	400Gb/s OSFP56 FR4 2km SMF Optical Transceiver

Absolute Maximum Ratings

Stress in excess of any of the individual Absolute Maximum Ratings can cause immediate catastrophic damage to the module even if all other parameters are within Recommended Operating Conditions. It should not be assumed that limiting values of more than one parameter can be applied to the module concurrently. Exposure to any of the Absolute Maximum Ratings for extended periods can adversely affect reliability.

Parameter	Symbol	Min	Typical	Max	Units	Notes
Storage Temperature	Ts	-40		85	°C	
3.3 V Power Supply Voltage	Vcc	-0.5	3.3	3.6	V	
Data Input Voltage - Single Ended		-0.5		Vcc+0.5	V	
Data Input Voltage - Differential				0.8	V	1
Relative Humidity	RH	5		95	%	

Note:

1. This is the maximum voltage that can be applied across the differential inputs without damaging the input circuitry. The damage threshold of the module input shall be at least 1600 mV peak to peak differential.

Recommended Operating Conditions

For operations beyond the recommended operating conditions, optical and electrical characteristics are not defined, reliability is not implied, and such operations for a long time may damage the module.

Parameter	Symbol	Min	Typical	Max	Units	Notes
Operating case temperature	Tc	0		70	°C	1
Storage temperature	Ts	-40		+85	°C	
Power supply voltage	Vcc	3.135	3.3	3.465	V	
Power dissipation	P_D			8	W	
Electrical Signal Rate per Channel (PAM encoded)			26.5625		GBd	2
Optical Signal Rate per Channel (PAM encoded)			53.125		GBd	3
Power Supply Noise				66	mVpp	4
Receiver Differential Data Output Load			100		Ohm	
Fiber Length (9um SMF)				2	km	5

Note:

1. 400GAUI-8 operation with Host generated FEC. The transmitter must receive pre-coded FEC signals from the host ASIC.

2. 400G FR4 operation with Host generated FEC. The transmitter must receive pre-coded FEC signals from the host ASIC.

3. Power Supply Noise is defined as the peak-to-peak noise amplitude over the frequency range at the host supply side of the recommended power supply filter with the module and recommended filter in place. Voltage levels including peak-to-peak noise are limited to the recommended operating range of the associated power supply. See Figure 7 for recommended power supply filter.

4. 9μm SMF. The maximum link distance is based on an allocation of 1dB of attenuation and 3dB total connection and splice loss. The loss of a single connection shall not exceed 0.5dB.

Electrical Characteristics

Unless otherwise stated, the following characteristics are defined under recommended operating conditions.

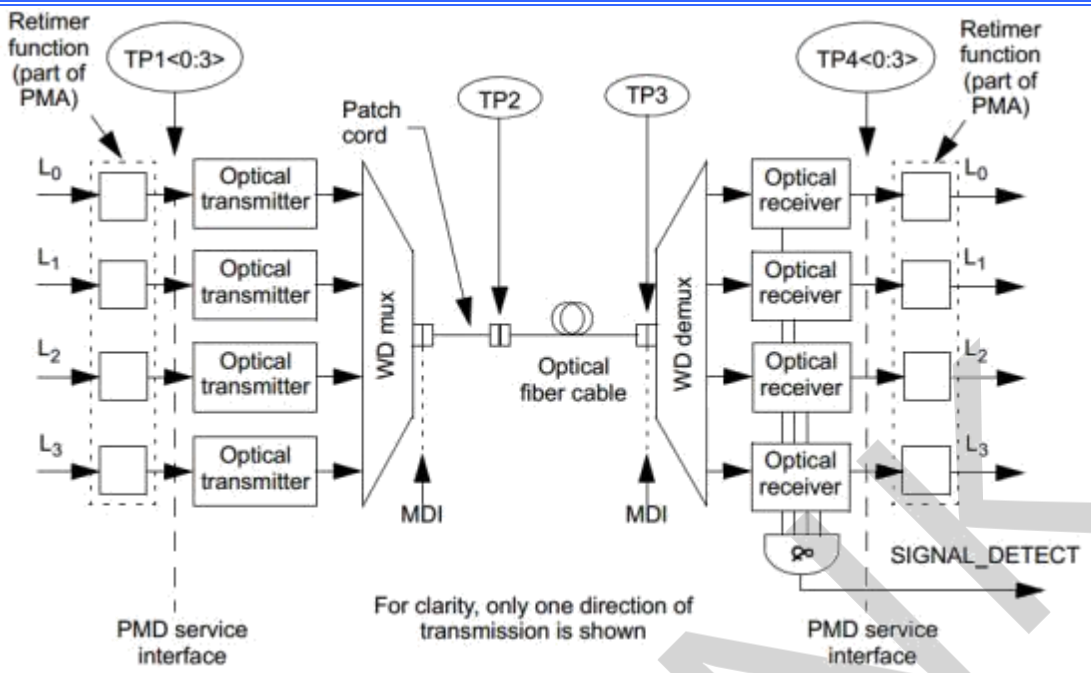
Parameter	Symbol	Min	Typical	Max	Units	Notes
Transceiver Power Consumption				8	W	
Transceiver Power Supply Current, Total				2550	mA	
AC coupling capacitors (Internal)			0.1		uF	

Note:

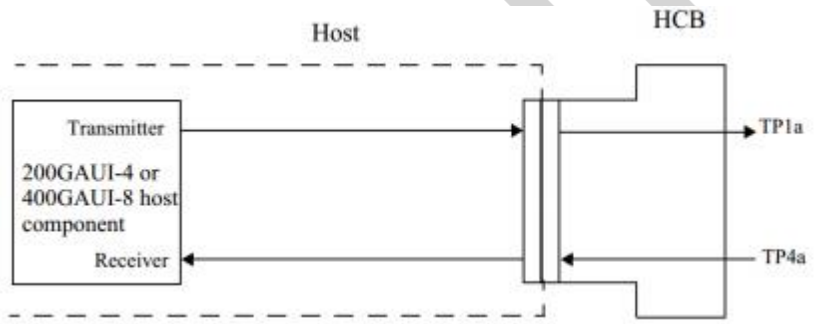
1. For control signal timing including LPWn/PRSn, INT/RSTn, SCL and SDA see Control Interface Section

Reference Points

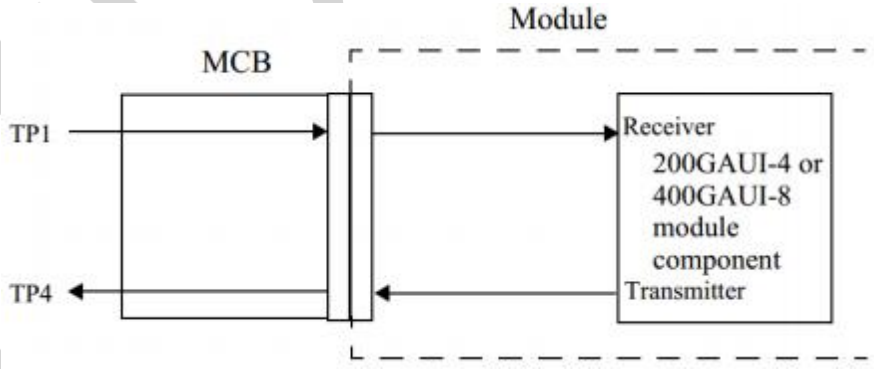
Test Point	Description
TP0 to TP5	The channel including the transmitter and receiver differential controlled impedance printed circuit board insertion loss and the cable assembly insertion loss.
TP1 to TP4	All cable assembly measurements are made between TP1 and TP4 as illustrated in Figure 3.
TP0 to TP2 TP3 to TP5	A mated connector pair has been included in both the transmitter and receiver specifications defined in 802.3ck 162.9.3 and 162.9.4. The recommended maximum insertion loss from TP0 to TP2 or from TP3 to TP5 including the test fixture is provided in 802.3ck 162.9.3.2
TP2	Unless specified otherwise, all transmitter measurements defined in 802.3-2022 151.7.1 are made at TP2 utilizing the test fixture specified in Annex 120E.
TP3	Unless specified otherwise, all receiver measurements and tests defined in 802.3-2022 151.7.12 are made at TP3 utilizing the test fixture specified in Annex 120E.



IEEE 802.3-2022 400GBASE-FR4 and 400GBASE-LR4 link



IEEE 802.3bs host compliance points TP1a, TP4a



IEEE 802.3bs module compliance points TP1, TP4

High Speed Electrical Input Characteristics

The following characteristics are defined over the Recommended Operating Conditions unless otherwise noted.

Parameter	Test Point	Typical	Min.	Max.	Unit	Conditions
Signaling Rate, Per Lane (PAM4 encoded)	TP1		26.5625		GBd	+/- 100 ppm

Differential peak-peak Input Voltage Tolerance	TP1a		900		mV	
Differential-mode to common-mode return loss	TP1		Equation (83E-6)		dB	802.3bs 120E.3.4
Differential termination mismatch	TP1			10	%	
Module stressed input tolerance	TP1a		See 120E.3.4.1			802.3bs 120E.3.4
Single-ended voltage tolerance range	TP1a		-0.4	3.3	V	
DC common-mode voltage tolerance range	TP1		-350	2850	mV	
	Module stressed input tolerance test :					
Applied peak-peak sinusoidal jitter		Table 120E-6		802.3bs 120E.3.4.1		
	Eye height 32			mV	802.3bs 120E.3.4.1	

High Speed Electrical Output Characteristics

The following characteristics are defined over the Recommended Operating noted.

Parameter	Test Point	Min.	Typical	Max.	Unit	Note
Signaling Rate, Per Lane (range)	TP4		26.5625 ± 100 ppm		GBd	1
AC common-mode output voltage	TP4			17.5	mV	
Differential peak-to-peak input voltage(min)	TP4			900	mV	
Eye height	TP4	30			mV	
Common-mode to differential-mode return loss	TP4	Equation (83E-3)			dB	
Differential termination mismatch	TP4			10	%	
Transition time	TP4	9.5			ps	
DC common-mode voltage tolerance	TP4	-0.35		2.85	V	

Note:

1. The signaling rate range is derived from the PMD receiver input.

High Speed Optical Transmitter Characteristics

The following characteristics are defined over the Recommended Operating Conditions unless otherwise noted.

Optical Characteristics @TP2 Test Point

Parameter	Symbol	Min.	Typical	Max.	Unit	
Signaling speed per lane			53.125± 100ppm		GBd	
Modulation format			PAM4			
Lane_1 Center Wavelength	λ_{C0}	1264.5	1271	1277.5	nm	
Lane_2 Center Wavelength	λ_{C1}	1284.5	1291	1297.5	nm	
Lane_3 Center Wavelength	λ_{C2}	1304.5	1311	1317.5	nm	
Lane_4 Center Wavelength	λ_{C3}	1324.5	1331	1337.5	nm	
Side-mode Suppression Ratio	SMSR	30			dB	
Total average launch power				9.3	dBm	
Average launch power, each lane	TxAVG	-3.3		3.5	dBm	1
Outer Optical Modulation Amplitude (OMA_{outer}), each lane	TxOMA	-0.3		3.7	dBm	2
Difference in launch power between any two lanes (OMA_{outer})				4	dB	
Launch power in OMA_{outer} minus TDECQ, each lane: for extinction ratio ≥ 4.5 dB for extinction ratio < 4.5 dB		 -1.7 -1.6			dBm	
Transmitter and dispersion eye closure for PAM4 (TDECQ) , each lane	TDECQ			3.4	dB	
TDECQ – 10*$\log_{10}$ (Ceq), each lane				3.4	dB	
| TDECQ-TECQ |				2.5	dB	
Average launch power of OFF transmitter, each lane				-30	dBm	
Extinction Ratio	ER	3.5			dB	
Transmitter transition time				17	ps	
$RIN_{17.1}$ OMA				-136	dB/Hz	
Optical return loss tolerance				17.1	dB	
Transmitter reflectance				-26	dB	

Note:

1. Average launch power, each lane (min) is informative and not the principal indicator of signal strength. A transmitter with launch power below this value cannot be compliant; however, a value above this does not ensure compliance.

2. Even if the TDECQ < 1.4 dB for an extinction ratio of ≥ 4.5 dB or TDECQ < 1.3 dB for an extinction ratio of < 4.5 dB, the OMA_{outer} (min) must exceed this value.

3. Transmitter reflectance is defined looking into the transmitter

Optical and Characteristics

Parameter	Symbol	Min.	Typical	Max.	Unit	
Signaling speed per lane			53.125±100ppm		GBd	
Modulation format			PAM4			
Lane_1 Center Wavelength	λ_{C0}	1264.5	1271	1277.5	nm	
Lane_2 Center Wavelength	λ_{C1}	1284.5	1291	1297.5	nm	
Lane_3 Center Wavelength	λ_{C2}	1304.5	1311	1317.5	nm	
Lane_4 Center Wavelength	λ_{C3}	1324.5	1331	1337.5	nm	
Damage threshold each lane		5.4			dBm	1
Average receive power each lane	RxAVG	-7.3		3.5	dBm	2
Receive Power (OMA_{outer}) each lane	RxOMA			3.7	dBm	
Difference in receive power between any two lanes (OMA_{outer})				4.1	dB	
Receiver reflectance				-26	dB	
Receiver sensitivity (OMA_{outer}), each lane for TDECQ<1.4dB for 1.4dB<TECQ<3.4dB	SenOMA			 -4.6 TECQ-6.0	dBm	3
LOS Assert	LOSA	-15			dBm	
LOS De-Assert	LOSD			-10	dBm	
LOS Hysteresis dB					0.5	

Note:

1. The receiver shall be able to tolerate, without damage, continuous exposure to an optical signal having this average power level. The receiver does not have to operate correctly at this input power.

2. Average receive power, each lane (min) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.

3. Measured with conformance test signal at TP3 for the BER specified in IEEE 802.3-2022 clause 151.7.12.

Pin Diagram

Pin Definitions

Pin	Logic	Symbol	Description	Plug Sequence	Notes
1		GND	Ground	1	1
2	CML-I	Tx2p	Transmitter Data Non-Inverted	3	
3	CML-I	Tx2n	Transmitter Data Inverted	3	
4		GND	Ground	1	1
5	CML-I	Tx4p	Transmitter Data Non-Inverted	3	
6	CML-I	Tx4n	Transmitter Data Inverted	3	
7		GND	Ground	1	1
8	CML-I	Tx6p	Transmitter Data Non-Inverted	3	
9	CML-I	Tx6n	Transmitter Data Inverted	3	
10		GND	Ground	1	1
11	CML-I	Tx8p	Transmitter Data Non-Inverted	3	
12	CML-I	Tx8n	Transmitter Data Inverted	3	
13		GND	Ground	1	1
14	LVCMO S-	SCL	2-wire Serial interface clock	3	2

	I/O				
15		VCC	+3.3V Power	2	
16		VCC	+3.3V Power	2	
17	Multi-Level	LPWn/PRSn	Low-Power Mode/Module Present	3	
18		GND	Ground	1	1
19	CML-O	Rx7n	Receiver Data Inverted	3	
20	CML-O	Rx7p	Receiver Data Non-Inverted	3	
21		GND	Ground	1	1
22	CML-O	Rx5n	Receiver Data Inverted	3	
23	CML-O	Rx5p	Receiver Data Non-Inverted	3	
24		GND	Ground	1	1
25	CML-O	Rx3n	Receiver Data Inverted	3	
26	CML-O	Rx3p	Receiver Data Non-Inverted	3	
27		GND	Ground	1	1
28	CML-O	Rx1n	Receiver Data Inverted	3	
29	CML-O	Rx1p	Receiver Data Non-Inverted	3	
30		GND	Ground	1	1
31		GND	Ground	1	1
32	CML-O	Rx2p	Receiver Data Non-Inverted	3	
33	CML-O	Rx2n	Receiver Data Inverted	3	
34		GND	Ground	1	1
35	CML-O	Rx4p	Receiver Data Non-Inverted	3	
36	CML-O	Rx4n	Receiver Data Inverted	3	
37		GND	Ground	1	1
38	CML-O	Rx6p	Receiver Data Non-Inverted	3	
39	CML-O	Rx6n	Receiver Data Inverted	3	
40		GND	Ground	1	1
41	CML-O	Rx8p	Receiver Data Non-Inverted	3	
42	CML-O	Rx8n	Receiver Data Inverted	3	
43		GND	Ground	1	1
44	Multi-Level	INT/RSTn	Module input/Module Reset	3	
45		VCC	+3.3V Power	2	
46		VCC	+3.3V Power	2	

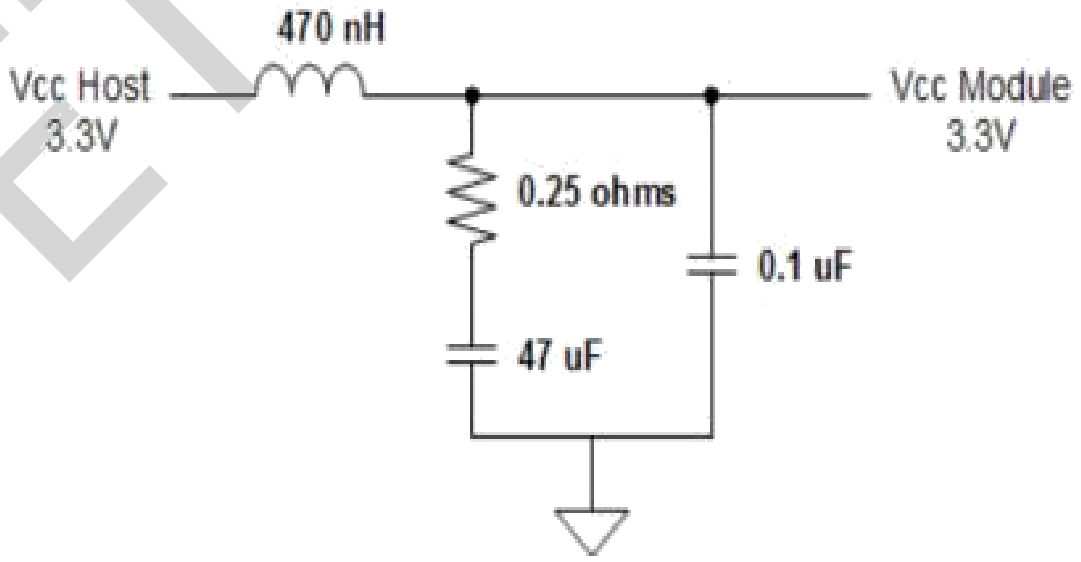
47	LVCMOS-I/O	SCL	2-wire Serial interface Data	3	2
48		GND	Ground	1	1
49	CML-I	Tx7n	Transmitter Data Inverted	3	
50	CML-I	Tx7p	Transmitter Data Non-Inverted	3	
51		GND	Ground	1	1
52	CML-I	Tx5n	Transmitter Data Inverted	3	
53	CML-I	Tx5p	Transmitter Data Non-Inverted	3	
54		GND	Ground	1	1
55	CML-I	Tx3n	Transmitter Data Inverted	3	
56	CML-I	Tx3p	Transmitter Data Non-Inverted	3	
57		GND	Ground	1	1
58	CML-I	Tx1n	Transmitter Data Inverted	3	
59	CML-I	Tx1p	Transmitter Data Non-Inverted	3	
60		GND	Ground	1	1

Note:

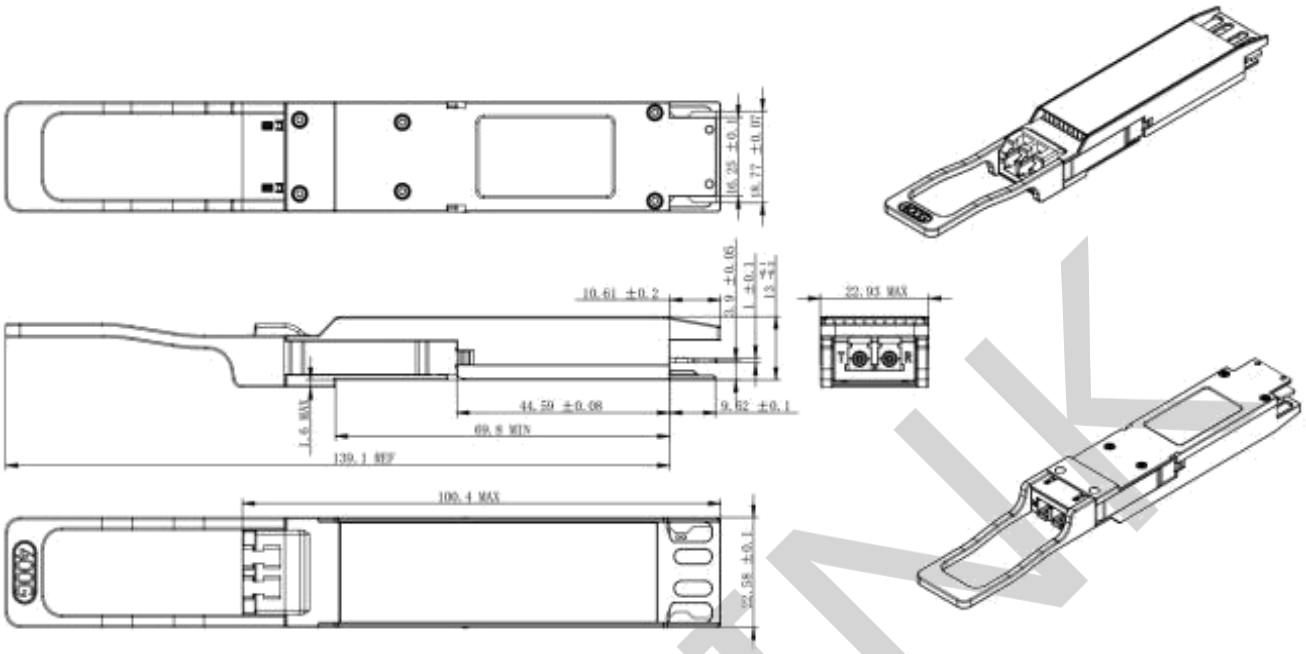
1. OSFP uses common ground (GND) for all signals and supply (power). All are common within the OSFP module and all module voltages are referenced to this potential unless otherwise noted.

2. Open-Drain with pull up resistor on Host.

Recommended Interface Circuit



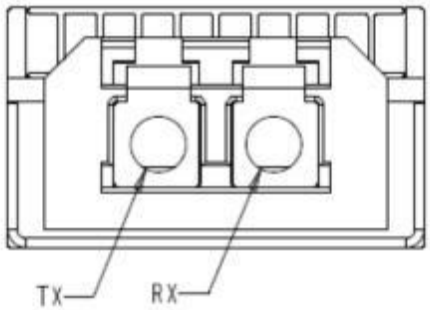
Mechanical Diagram



The bellow picture shows the location of the hottest spot for measuring module case temperature. In addition, the digital diagnostic monitors (DDM) temperature is also calibrated to this spot.

TBD

The optical interface port is a Duplex LC connector.



Module Optical Interface (looking into the optical port)

Revision History

Version No.	Date	Description
1.0	February 18, 2023	Preliminary datasheet
2.0	July 28,2024	Product upgrades

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